CLAIMS

1. An apparatus comprising:

a first circuit configured to generate a plurality of control signals and a select signal, in response to (i) a receive clock signal, (ii) a reference clock signal and (iii) a master clock signal;

a second circuit configured to generate a read signal and a window signal in response to said plurality of control signals; and

a third circuit configured to generate a lock signal in response to (i) said reference clock signal; (ii) said select signal; (iii) said read signal and (iv) said window signal, wherein said receive clock signal and said reference clock signal are independent clocks configured to provide range control over one or more channels.

2. The apparatus according to claim 1, wherein said apparatus is configured to provide proper operation for any combination of phase and frequency of said receive clock signal and said reference clock signal.

3. The apparatus according to claim 1, wherein said receive clock signal comprises a plurality of receive clock signals and said reference clock signal comprises a plurality of reference clock signals.

4. The apparatus according to claim 3, wherein said master clock signal comprises at least one of said plurality of reference clock signals.

5. The apparatus according to claim 1, wherein said third circuit is configured to determine if said receive clock signal and said reference clock signal are within a predetermined tolerance.

6. The apparatus according to claim 1, wherein said third circuit comprises a range control circuit.

7. The apparatus according to claim 1, wherein said second circuit is configured to perform a double synchronization handshake to eliminate metastability.

8. The apparatus according to claim 1, wherein said second circuit is configured to perform an asynchronous reset to prevent false reads.

9. The apparatus according to claim 1, wherein:

said first circuit comprises a master clock domain circuit configured to select (i) a channel and (ii) a receive clock and a reference clock for said channel, wherein said first circuit generates a reset signal and increments a channel select after acknowledgment that a lock decision for the selected channel has been completed;

said second circuit comprises a selected clock domain circuit configured to (i) receive said reset signal, (ii) present a read signal in the selected reference clock domain at a specific count and (iii) activate a window signal between two counts in the selected receive clock domain; and

said third circuit comprises a range control circuit configured to update the channel selected clock signal in response to said read signal, said window signal and said channel signal.

10. The apparatus according to claim 9, wherein:

said master clock domain circuit comprises a channel select circuit configured to generate said select signal and a hand shake circuit configured to generate one or more of said plurality of control signals;

said selected clock domain comprises one or more counters and one or more logic circuit configured to generate said read signal and said write signal; and

said range control circuit comprises one or more logic circuits and a register configured to present said lock signal.

11. The apparatus according to claim 9, wherein said selected clock domain circuit comprises:

a selected receive clock domain circuit configured to generate said window signal; and

a selected reference clock domain circuit configured to generate said read signal.

12. An apparatus comprising:

means for generating a plurality of control signals and a select signal, in response to (i) a receive clock signal, (ii) a reference clock signal and (iii) a master clock signal;

means for generating a read signal and a window signal in response to said plurality of control signals;

means for generating a lock signal in response to (i) said reference clock signal; (ii) said select signal; (iii) said read signal and (iv) said window signal; and

means for providing independent range control over one or more channels with said receive clock signal and said reference clock signal.

13. A method for providing independent roving range control, comprising the steps of:

(A) generating a plurality of control signals and a select signal, in response to (i) a receive clock signal, (ii) a reference clock signal and (iii) a master clock signal;

(B) generating a read signal and a window signal in response to said plurality of control signals; and

(C) generating a lock signal in response to (i) said reference clock signal; (ii) said select signal; (iii) said read signal and (iv) said window signal, wherein said lock signal provides independent range control between one or more channels of said receive clock signal and said reference clock signal.

14. The method according to claim 13 wherein said method provides proper operation for any combination of phase and frequency of said receive clock signal and said reference clock signal.

15. The method according to claim 13, wherein said receive clock signal comprises a plurality of receive clock signals and said reference clock signal comprises a plurality of reference clock signals.

16. The method according to claim 15, wherein said master clock signal comprises at least one of said plurality of reference clock signals.

17. The method according to claim 13, wherein step (C) further comprises:

determining if said receive clock signal and said reference clock signal are within a predetermined tolerance.

18. The method according to claim 13, wherein said step (B) further comprises:

performing a double synchronization handshake to eliminate metastability.

19. The method according to claim 13, wherein step (B) further comprises:

performing an asynchronous reset to prevent false reads.